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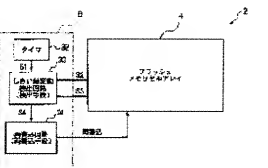
(54) NON-VOLATILE STORAGE DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To make compensating degradation of an electric charges holding characteristic easy with multi-values memory.
SOLUTION: This device has a detecting means 30 detecting variation of threshold voltage of a specific transistor (memory transistors and a reference transistor constituting memory cell 4), and a rewriting means 34 writing data again in the memory cell 4 when the means 30 detects variation of threshold. Specifically, the detecting means 30 detects whether it has threshold voltage at a detection place apart from the center by the prescribed voltage in the direction of one side or not for distribution in directly after writing threshold voltage. Also the detecting means 30 is provided with a timer 32 giving detection timing.



* NOTICES *

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3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1]A nonvolatile storage which made data which can be written in each memory cell by having the memory transistor characterized by comprising the following provided with a charge storage layer for every memory cell, changing the amount of injected charges to a charge storage layer, and adjusting threshold voltage of a memory transistor more than ternary.
A detection means to detect change of threshold voltage of a specific transistor.
A rewrting means to perform data writing for the second time to a memory cell when this detection means detects change of threshold voltage of a specific transistor.

[Claim 2]The nonvolatile storage according to claim 1 which said detection means is the detection part where only prescribed voltage got used to one side to distribution immediately after writing of the threshold voltage about a specific transistor, and detects change of threshold voltage by whether it has threshold voltage in this detection part.
[Claim 3]The nonvolatile storage according to claim 1 which has further a timer for giving timing which detects change of threshold voltage to said detection means.
[Claim 4]The nonvolatile storage according to claim 1 in which said charge storage layer is an insulating layer.
[Claim 5]The nonvolatile storage according to claim 1 with which stored charge which a tunnel oxide film is made to have intervened between said charge storage layer and a semiconductor substrate, and has been poured into said charge storage layer changes inside of this tunnel oxide film by direct tunneling.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to nonvolatile storages, such as rewritable semiconductor memory, for example, EEPROM, and a flash EEPROM, electrically.
[0002]
[Description of the Prior Art]It has a charge storage layer which consists of a flow FINGU gate or an insulator layer between a control gate and a semiconductor substrate, and the memory transistor comprises semiconductor memory, such as EEPROM and a flash EEPROM. And he is trying to distinguish stored data by writing in data and reading the current from the storage states of the electron in the written-in memory transistor by generally pouring an electron into this charge storage layer.
[0003]Therefore, these things [guaranteeing the charge storage characteristic after a data rewrite with a rewritable nonvolatile storage electrically] are dramatically important on the reliability of a product. On the other hand, in a flash EEPROM. Since threshold voltage is verified for every bit from the first and it controls precisely, it is easy to multiple-value-ize threshold voltage of the memory transistor of each cell, and the motion which multiple-value-izes this kind of memory, and attains effectual high integration has recently been activating.
[0004]
[Problem(s) to be Solved by the Invention]However, in the multiple-value-ized nonvolatile storage (henceforth a multi level memory) of this former. For example, there is nothing provided with the refresh function for guaranteeing a charge storage characteristic like DRAM, and, for this reason, it is becoming difficult with the minuteness making of a memory transistor, especially thin-film-izing of a tunnel oxide film to guarantee a charge storage characteristic over a long period of time.
[0005]Drawing 5 is a figure showing the holding property of the electric charge accumulated into the silicon nitride film about the MONOS (Metal OxideNitride Oxide Semiconductor) type flash EEPROM which used the silicon nitride film as a charge storage layer. A horizontal axis shows among a figure the time which impressed stress thermally, and the vertical axis shows the threshold voltage Vth of the memory transistor. The thickness of a middle silicon nitride film and the upper silicon oxide film sets to 8.3 nm and 4 nm, respectively, and makes the parameter thickness t_{ox} of the tunnel oxide film made to intervene between a silicon nitride film and a semiconductor substrate.
[0006]As for the memory transistor first set as positive voltage, and the memory transistor set as negative voltage at the beginning, mutual threshold voltage approaches with progress of stress applying time so that drawing 5 may show. This reflects the phenomenon from which the electron held in the silicon nitride film as a charge storage layer escapes outside. Generally it is explained that this phenomenon originates in the increase in leakage current of the tunnel oxide film resulting from stress according to a heat-dissipation model in addition to an electric charge carrying out spontaneous emmision in connection with the passage of time. With progress of minuteness making,

change of threshold voltage is also sharp and the situation where it becomes increasingly severe clearing ten years which are the present minimum term of a guarantee will be expected from now on (so that thickness t_{ox} of a tunnel oxide film specifically becomes thin). In order to raise the interfacial characteristic of a tunnel oxide film and the silicon nitride film by a CVD method like a graphic display, Heating processes, such as RTN (Rapid Thermal Nitrization) beforehand performed after membrane formation of a tunnel oxide film, also show that a charge storage characteristic deteriorates.

[0007]If degradation of such a charge storage characteristic becomes remarkable, the distinction margin of data falls, and since it is changed into other data, in the severe case where distinction of data cannot be performed, the reliability of a memory will be spoiled remarkably. Although degradation of this charge storage characteristic is a common problem which does not ask whether the data of a memory is a binary, or it is a multiple value, If it is especially in the case of a multi level memory and multiple-value-ization is advanced, the influence which degradation of a charge storage characteristic has on read-out (data distinction) of a memory still further from distribution of threshold voltage approaching mutually from the time of a binary so much will become large.

[0008]This invention is made in view of such the actual condition, and newly proposes the technique of degradation compensation of a charge storage characteristic of having been suitable for the multi level memory, and an object of this invention is to provide the nonvolatile storage of a multiple value using this.

[0009]

[Means for Solving the Problem]Solve a problem of conventional technology mentioned above and to achieve the above objects with a nonvolatile storage (multi level memory) which this invention multiple-value-ized. It has a detection means to detect change of threshold voltage of a specific transistor, and a rewrting means to perform data write for the second time to a memory cell when this detection means detects change of threshold voltage of a specific transistor.

[0010]A rewrite of this data once eliminates stored data, and usually performs it by writing in an initial data again. In especially a multi level memory, without performing elimination of stored data, since threshold voltage can be verified for every bit and it can usually control precisely, it is also possible to return data so that a changed part of threshold voltage of a memory transistor may be compensated. These can perform degradation compensation of a charge storage characteristic easily.

[0011]Since just set-up threshold voltage will specifically fall if an electron falls out when stored charge is an electron, for example, it is good to detect the change at the negative voltage side of threshold distribution of voltage. That is, a detection means in this case is the detection part where only prescribed voltage got used to one side to distribution immediately after writing of that threshold voltage about a specific transistor, and is characterized [other] by detecting change of threshold voltage by whether it has threshold voltage in this detection part.

[0012]Change detection of threshold voltage is performed periodically, and also it may carry out non-periodically according to time no rewriting to be, for example or the number of times of rewriting. Processing of in any case, shortening fixed time according to measurement of time neither fixed time nor rewriting to be or the number of times of rewriting, if detection timing is given by an internal timer can be performed.

[0013]Since degradation of a charge storage characteristic is intense compared with a case where this is a conducting film when charge storage layers are insulator layers, such as a silicon nitride film, for example, an effect of degradation compensation by application of this invention is large. For voltage lowering, stored charge is good to make inside of a tunnel oxide film change by direct tunneling.

[0014]

[Embodiment of the Invention]The nonvolatile storage of this invention can perform rewriting of data electrically, and are the nonvolatile memory in which multiple-value-izing is possible, for example,

EEPROM, a flash EEPROM, etc. so that clearly also from the above explanation.
[0015]Hereafter, a flash EEPROM is explained in detail as an example of the nonvolatile storage concerning this invention based on a drawing. Drawing 1 is an outline lineblock diagram showing the important section about the flash EEPROM concerning this invention. The circuit diagram which drawing 2 expands a part of NOR type flash memory cell array, and is shown, and drawing 3 are the abbreviated section structure figures of the memory transistor which constitutes this memory cell array.
[0016]General classification of this flash EEPROM 2 constitutes it from the flash memory cell array 4 which comprised many memory cells, and the peripheral circuit 6 for writing in and reading [eliminate and] data to this memory cell array 4, as shown in drawing 1. The graphic display here is constituted by the peripheral circuit 6 including a sense amplifier, an input-and-output control circuit, a clock generation circuit, etc. besides various kinds of decoders or a buffer circuit, although omitted. The verification circuit for usually writing data in the memory cell array 4 correctly is also included in many cases.
[0017]The limitation in particular of two flash EEPROM concerning this invention may not be in the cell method, and it may be which cell methods, such as a NAND type and a DINOR (DIvided bit line NOR) type, besides a NOR type. When the circuitry of the concrete memory cell array 4 is explained in the NOR type shown, for example in drawing 2, to this memory cell array 4. Much memory transistor MTm-1, n-1, MTm-1, n, MTm-1, n+1, MTm, n-1, MTm, n, MTm, n+1, MTm+1, n-1, MTm+1, n, MTm+1, and n+1 are arranged at matrix form. And interconnection of these memory transistors is carried out to a transverse direction by word line WLm-1, WLm, and WLm+1, and interconnection is carried out to the lengthwise direction with bit line BLn-1, BLn, BLn+1, and the common source line SRL.
[0018]Each memory transistor in this invention has been arranged for every memory cell, and is provided with the charge storage layer which accumulates stored data as an electric charge, respectively. It is multiple-value-ized by making the data which can be written in each memory cell more than ternary by changing the amount of injected charges of this charge storage layer, and having adjusted the threshold voltage of a memory transistor.
[0019]As a charge storage layer, whether they are conductive layers, such as a floating gate, a MONOS (Metal Oxide Nitride Oxide Semiconductor) type, There is no limitation in the construction material regardless of whether it is an insulating layer like the MNOS (Metal Nitride Oxide Semiconductor) type which omitted the upper layer insulation film.
[0020]Hereafter, in the MONOS type shown, for example in drawing 3, the composition of the concrete memory transistor is explained briefly. Among drawing 3, the semiconductor substrate which the numerals 10 introduced the p type impurity, for example, and was electric-conduction-ized is shown, and the gate electrode 14 is formed in the surface of this semiconductor substrate 10 via the ONO (Oxide Nitride Oxide) film 12. ONO film 12 comprises a lower layer oxide film (tunnel oxide film 16) by the side of a substrate face, a middle nitride (silicon nitride film 18), and the upper oxide film 20. As for the thickness of the tunnel oxide film 16, although there is no limitation in particular, it is desirable to make degradation of data holding characteristics thinner than 4 nm in a meaning, such as to keep step with a direction on the other hand, so that it may explain in full detail later. In this MONOS type, it functions as a charge storage layer which the middle silicon nitride film 18 described above, and an electric charge is accumulated in this trap. The gate electrode 14 comprises a polycide film etc. which, for example, made the silicide film (for example, WSi) laminate on a polysilicon film and a polysilicon film.
[0021]The sidewall 22 which consists of silicon oxide films etc., for example is formed in the both sides of ONO film 12 and the gate electrode 14. The low-concentration impurity diffusion region (n^- field 24) called LDD, respectively is shallowly formed in the substrate face side applied outside from the both edges of the tunnel oxide film 16. On the other hand, the high-concentration impurity

diffusion region (n^+ field 26) called sauce or a drain area, respectively is deeply formed in the substrate back side applied outside from the rim of the sidewall 22.

[0022]Although not illustrated in particular, on this, multilevel interconnection of the wiring layers, such as aluminum, is carried out via a layer insulation layer, and the gate electrode 14, sauce, or the n^+ field 26 as a drain area is connected to this multilevel interconnection. Thereby, the interconnection of the memory transistor by word line WLm−1 shown in drawing 2, WLm, WLm+1, bit line BLn−1, BLn, BLn+1, and the common source line SRL is made.

[0023]In such a MONOS type memory transistor of composition, the depression transistor by which the channel was formed in the substrate face on both sides of the tunnel oxide film 16 at the time of no bias is used. The data writing impresses predetermined bias to the gate electrode 14 or the n^+ field 26, and is performed. For example, if pulse voltage is impressed to the word line WLm and the bit line BLn on conditions which were illustrated to drawing 2 when writing data in the central memory transistor MTm and n, an electric charge (in this case, electron) will be supplied to the n^+ field 26 of drawing 3 from the common source line SRL. And the electron which had inside of a channel accelerated is becoming a channel hot electron (CHE) in the pinch−off field near the drain, and running through the tunnel oxide film 16, and after being poured into the silicon nitride film 18 as a charge storage layer, it is accumulated in the trap. The amount of charge storages is decided by the voltage and applying time of pulse voltage.

[0024]According to this amount of charge storages, the threshold voltage Vth of a memory transistor shifts to a right side, and a memory transistor changes to an enhancement mode. As mentioned above, the memory transistor concerning this invention is multiple−value−ized more than ternary. Drawing 4 illustrates the case where the data of four values is memorized in a memory transistor. This figure is a distribution map of the threshold voltage Vth in the memory cell array 4, and a horizontal axis shows the number (frequency) of the memory transistor in which Vth of a vertical axis is the same for Vth.

[0025]If the memory transistor group of the depletion mode in which the electric charge is not accumulated is set to "0" like a graphic display, the memory transistor group "1" of an enhancement mode, "2", and "3" are discretely distributed in order in the direction to which the amount of charge storages increases and Vth becomes high. Usually, in order to make distinction of data easy, like a graphic display, the keepout area of writing is set up between each distribution, and data writing is performed with the margin to this keepout area. Thus, the writing (adjustment of the amount of stored charge) of exact data is attained by carrying out close control of the Vth by said verification circuit in the case of the above−mentioned data writing, verifying the value.

[0026]On the other hand, the bottom of the predetermined bias condition which is not illustrated in particular in this NOR type cell at the time of that data erasure and stored charge are FN(s) (Fowler Nordheim). It is drawn out by the tunnel ring. By the way, as previously pointed out as a problem of conventional technology, by drawing 5 in EEROM. When the electric charge once accumulated in the charge storage layer (for example, silicon nitride film 18) is neglected for a long time, according to a heat−dissipation model, it escapes to the substrate side gradually by stress, and there is a problem that a charge storage characteristic deteriorates.

[0027]In order to cope with this problem, it has some means for compensating this characteristic degradation, and comprises the flash EEPROM 2 concerning this invention. Namely, as shown in drawing 1, in the peripheral circuit 6, The threshold fluctuation detecting circuit 30 as a detection means to detect change of the threshold voltage Vth of a memory transistor, The timer 32 for this threshold fluctuation detecting circuit 30 to give the timing which detects change of Vth, When the threshold fluctuation detecting circuit 30 detects Vth change of a memory transistor, the rewrting circuit 34 as a rewrting means to perform data writing for the second time to a memory cell is formed.

[0028]when operation of this degradation compensation was explained in more detail, the detection

timing signal S1 which directs change detection of Vth to the threshold fluctuation detecting circuit 30 called it once from the timer 32 first in the moon, for example -- it is outputted periodically or un-periodically. Whenever it switches on a power supply, for example, it is made to make the detection timing signal S1 output as an example in the case of being un-periodical, or the existence of rewriting is supervised, and when time no rewriting to be exceeds predetermined time, it may be made to make the detection timing signal S1 output. Store beforehand in the memory the table showing a relation with the longest charge holding time (marginal retention time) that serves as rewriting frequency and a limit of data distinction, for example, and the frequency of rewriting is supervised, If rewriting frequency is large, the detection timing signal S1 will be made to output a little early, and as long as rewriting frequency is small, it may be made to delay the stage to which the detection timing signal S1 is made to output, referring to the read table. You may make it control the processings in these cases of being un-periodical (surveillance about a power supply or rewriting, read-out of a table, etc.) not only by the timer 32 side but by the threshold fluctuation detecting circuit 30 side. In this case, the detection timing signal S1 is a signal of a hour entry.

[0029]By the input of the detection timing signal S1, the threshold fluctuation detecting circuit 30 performs change detection of the threshold voltage Vth of the specific transistor to the memory cell array 4. That is, as shown in drawing 2, the detection start signal S2 is outputted to a specific transistor, and change of the Vth is inputted as the detecting signal S3.

[0030]The reference cell which receives stress equivalent to a memory cell concrete, for example is beforehand provided in the memory cell array 4, and Vth of the reference transistor is seen whether have shifted or not. When the area of the memory cell array 4 is large, a reference cell may be provided for every block which constitutes the memory cell array 4, for example, or word line sector. It may be made to detect a gap of Vth about a regular memory transistor, without providing a reference cell. Specification of the regular memory cell to detect is arbitrary like arrangement of a reference cell.

[0031]Since Vth is shifted to a negative side because stored charge (electron) falls out in order to detect a gap of this Vth, As shown in drawing 4, to threshold distribution of voltage "1", "2", and "3", the detection part of deltaVth width is set to that negative voltage side, and the existence of the specific transistor with which Vth enters in this prescribed width is detected. This detection part is arbitrary, and although it may set up to which threshold distribution of voltage, since it is thought that the amount of change of the distribution "3" by the side of high Vth with many amounts of stored charge is large, generally it is good to set and set prescribed distance to the negative voltage side of the distribution "3" by the side of high Vth. The position of the detection part over Vth distribution can be provided in the positive voltage side edge of a keepout area, for example like a graphic display, although there is no limitation in particular.

[0032]Thus, if it judges that Vth change had the threshold fluctuation detecting circuit 30, from the threshold fluctuation detecting circuit 30, rewrting start signal S4 will be outputted to the rewrting circuit 34. The rewrting circuit 34 which inputted rewrting start signal S4 applies the re-writing of data to the memory cell array 4, as shown in drawing 1.

[0033]Although this re-writing may follow all the memory cells, it may follow only some memory cells. For example, when monitoring a reference cell, only about the memory cell of the circumference of a reference cell with Vth change, it is prescribed units, such as a block and a word line sector, and the re-writing of data may be performed. In the case where a regular memory cell is monitored, only the monitored memory cell besides a prescribed unit may perform the re-writing of data.

[0034]Stored data is once eliminated and the re-writing of this data is usually performed by writing in an initial data again. There is also the method of performing without eliminating stored data. That is, since threshold voltage can be verified for every bit and it can usually control by a multi level memory precisely, it is also possible to return data so that the changed charge quantity of the threshold voltage of a memory transistor may be compensated without performing elimination of

stored data. These data re-writing can perform degradation compensation of a charge storage characteristic easily.

[0035]Thus, since degradation of a charge storage characteristic is intense compared with the case where a charge storage layer is a conducting film in the MONOS type (or MNOS type) whose charge storage layers are insulator layers, such as a silicon nitride film, the effect of the degradation compensation by application of this invention is large. This invention is not limited to the above-mentioned explanation.

[0036]For example, in the above-mentioned explanation, the cell method illustrated the case where it had a MONOS type memory transistor with a NOR type, and it was presupposed that electric charge pouring is based on a channel hot electron (CHE). However, electric charge pouring according to NF tunneling with a NAND type or a DINOR type especially for reasons of low power consumption is also possible. Direct tunneling may be used for voltage lowering.

[0037]The thrust omission of the electric charge shifted to direct tunneling from NF tunneling, and this invention persons checked that the changing direction of Vth could be arranged with one side in the range in which the thickness is 3-4 nm, when thickness of the above mentioned tunnel oxide film 18 was made thinner than 4 nm. When an electron falls out, an electron hole does not go into a charge storage layer from the substrate side, and it is thought of because a depression field is not formed at the time of bias application for this reason that the changing direction of Vth can be arranged with one side in this thickness range.

[0038]This means that Vth change of the distribution "0" by the side of low Vth is almost lost by drawing 4. Since this is in agreement with the compensation direction of threshold voltage also for the surrounding memory cell if the changing direction of threshold voltage is beforehand arranged with one side even if there is what is called soft light in which the memory cell connected to the circumference on the occasion of data writing receives influence, it is desirable in this meaning.

[0039]

[Effect of the Invention]As explained above, according to the nonvolatile storage concerning this invention, in a multi level memory, degradation compensation of a charge storage characteristic can be performed easily. As a result, it multiple-value-ized, substantial high integration was attained, and it became possible to provide a reliable nonvolatile storage moreover.

[Translation done.]

TECHNICAL FIELD

[Field of the Invention]This invention relates to nonvolatile storages, such as rewritable semiconductor memory, for example, EEPROM, and a flash EEPROM, electrically.

[Translation done.]

PRIOR ART

[Description of the Prior Art]It has a charge storage layer which consists of a flow FINGU gate or an insulator layer between a control gate and a semiconductor substrate, and the memory transistor comprises semiconductor memory, such as EEPROM and a flash EEPROM. And he is trying to distinguish stored data by writing in data and reading the current from the storage states of the electron in the written-in memory transistor by generally pouring an electron into this charge storage layer.
[0003]Therefore, these things [guaranteeing the charge storage characteristic after a data rewrite with a rewritable nonvolatile storage electrically] are dramatically important on the reliability of a product. On the other hand, in a flash EEPROM. Since threshold voltage is verified for every bit from the first and it controls precisely, it is easy to multiple-value-ize threshold voltage of the memory transistor of each cell, and the motion which multiple-value-izes this kind of memory, and attains effectual high integration has recently been activating.

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EFFECT OF THE INVENTION

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However, in the multiple-value-ized nonvolatile storage (henceforth a multi level memory) of this former. For example, there is nothing provided with the refresh function for guaranteeing a charge storage characteristic like DRAM, and, for this reason, it is becoming difficult with the minuteness making of a memory transistor, especially thin-film-izing of a tunnel oxide film to guarantee a charge storage characteristic over a long period of time.
[0005]Drawing 5 is a figure showing the holding property of the electric charge accumulated into the silicon nitride film about the MONOS (Metal OxideNitride Oxide Semiconductor) type flash EEPROM which used the silicon nitride film as a charge storage layer. A horizontal axis shows among a figure the time which impressed stress thermally, and the vertical axis shows the threshold voltage Vth of the memory transistor. The thickness of a middle silicon nitride film and the upper silicon oxide film sets to 8.3 nm and 4 nm, respectively, and makes the parameter thickness t_{ox} of the tunnel oxide film made to intervene between a silicon nitride film and a semiconductor substrate.
[0006]As for the memory transistor first set as positive voltage, and the memory transistor set as negative voltage at the beginning, mutual threshold voltage approaches with progress of stress applying time so that drawing 5 may show. This reflects the phenomenon from which the electron held in the silicon nitride film as a charge storage layer escapes outside. Generally it is explained that this phenomenon originates in the increase in leakage current of the tunnel oxide film resulting from stress according to a heat-dissipation model in addition to an electric charge carrying out spontaneous emmision in connection with the passage of time. With progress of minuteness making, change of threshold voltage is also sharp and the situation where it becomes increasingly severe clearing ten years which are the present minimum term of a guarantee will be expected from now on (so that thickness t_{ox} of a tunnel oxide film specifically becomes thin). In order to raise the interfacial characteristic of a tunnel oxide film and the silicon nitride film by a CVD method like a graphic display, Heating processes, such as RTN (Rapid Thermal Nitrization) beforehand performed after membrane formation of a tunnel oxide film, also show that a charge storage characteristic deteriorates.
[0007]If degradation of such a charge storage characteristic becomes remarkable, the distinction margin of data falls, and since it is changed into other data, in the severe case where distinction of data cannot be performed, the reliability of a memory will be spoiled remarkably. Although degradation of this charge storage characteristic is a common problem which does not ask whether the data of a memory is a binary, or it is a multiple value, If it is especially in the case of a multi level memory and multiple-value-ization is advanced, the influence which degradation of a charge storage characteristic has on read-out (data distinction) of a memory still further from distribution of threshold voltage approaching mutually from the time of a binary so much will become large.
[0008]This invention is made in view of such the actual condition, and newly proposes the technique of degradation compensation of a charge storage characteristic of having been suitable for the multi level memory, and an object of this invention is to provide the nonvolatile storage of a multiple value

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[Translation done.]

MEANS

[Means for Solving the Problem]Solve a problem of conventional technology mentioned above and to achieve the above objects with a nonvolatile storage (multi level memory) which this invention multiple-value-ized. It has a detection means to detect change of threshold voltage of a specific transistor, and a rewrting means to perform data write for the second time to a memory cell when this detection means detects change of threshold voltage of a specific transistor.
[0010]A rewrite of this data once eliminates stored data, and usually performs it by writing in an initial data again. In especially a multi level memory, without performing elimination of stored data, since threshold voltage can be verified for every bit and it can usually control precisely, it is also possible to return data so that a changed part of threshold voltage of a memory transistor may be compensated. These can perform degradation compensation of a charge storage characteristic easily.
[0011]Since just set-up threshold voltage will specifically fall if an electron falls out when stored charge is an electron, for example, it is good to detect the change at the negative voltage side of threshold distribution of voltage. That is, a detection means in this case is the detection part where only prescribed voltage got used to one side to distribution immediately after writing of that threshold voltage about a specific transistor, and is characterized [other] by detecting change of threshold voltage by whether it has threshold voltage in this detection part.
[0012]Change detection of threshold voltage is performed periodically, and also it may carry out non-periodically according to time no rewriting to be, for example or the number of times of rewriting. Processing of in any case, shortening fixed time according to measurement of time neither fixed time nor rewriting to be or the number of times of rewriting, if detection timing is given by an internal timer can be performed.
[0013]Since degradation of a charge storage characteristic is intense compared with a case where this is a conducting film when charge storage layers are insulator layers, such as a silicon nitride film, for example, an effect of degradation compensation by application of this invention is large. For voltage lowering, stored charge is good to make inside of a tunnel oxide film change by direct tunneling.
[0014]
[Embodiment of the Invention]The nonvolatile storage of this invention can perform rewriting of data electrically, and are the nonvolatile memory in which multiple-value-izing is possible, for example, EEPROM, a flash EEPROM, etc. so that clearly also from the above explanation.
[0015]Hereafter, a flash EEPROM is explained in detail as an example of the nonvolatile storage concerning this invention based on a drawing. Drawing 1 is an outline lineblock diagram showing the important section about the flash EEPROM concerning this invention. The circuit diagram which drawing 2 expands a part of NOR type flash memory cell array, and is shown, and drawing 3 are the abbreviated section structure figures of the memory transistor which constitutes this memory cell array.

[0016]General classification of this flash EEPROM 2 constitutes it from the flash memory cell array 4 which comprised many memory cells, and the peripheral circuit 6 for writing in and reading [eliminate and] data to this memory cell array 4, as shown in drawing 1. The graphic display here is constituted by the peripheral circuit 6 including a sense amplifier, an input-and-output control circuit, a clock generation circuit, etc. besides various kinds of decoders or a buffer circuit, although omitted. The verification circuit for usually writing data in the memory cell array 4 correctly is also included in many cases.

[0017]The limitation in particular of two flash EEPROM concerning this invention may not be in the cell method, and it may be which cell methods, such as a NAND type and a DINOR (DIvided bit line NOR) type, besides a NOR type. When the circuitry of the concrete memory cell array 4 is explained in the NOR type shown, for example in drawing 2, to this memory cell array 4. Much memory transistor MTm-1, n-1, MTm-1, n, MTm-1, n+1, MTm, n-1, MTm, n, MTm, n+1, MTm+1, n-1, MTm+1, n, MTm+1, and n+1 are arranged at matrix form. And interconnection of these memory transistors is carried out to a transverse direction by word line WLm-1, WLm, and WLm+1, and interconnection is carried out to the lengthwise direction with bit line BLn-1, BLn, BLn+1, and the common source line SRL.

[0018]Each memory transistor in this invention has been arranged for every memory cell, and is provided with the charge storage layer which accumulates stored data as an electric charge, respectively. It is multiple-value-ized by making the data which can be written in each memory cell more than ternary by changing the amount of injected charges of this charge storage layer, and having adjusted the threshold voltage of a memory transistor.

[0019]As a charge storage layer, whether they are conductive layers, such as a floating gate, a MONOS (Metal Oxide Nitride Oxide Semiconductor) type, There is no limitation in the construction material regardless of whether it is an insulating layer like the MNOS (Metal Nitride Oxide Semiconductor) type which omitted the upper layer insulation film.

[0020]Hereafter, in the MONOS type shown, for example in drawing 3, the composition of the concrete memory transistor is explained briefly. Among drawing 3, the semiconductor substrate which the numerals 10 introduced the p type impurity, for example, and was electric-conduction-ized is shown, and the gate electrode 14 is formed in the surface of this semiconductor substrate 10 via the ONO (Oxide Nitride Oxide) film 12. ONO film 12 comprises a lower layer oxide film (tunnel oxide film 16) by the side of a substrate face, a middle nitride (silicon nitride film 18), and the upper oxide film 20. As for the thickness of the tunnel oxide film 16, although there is no limitation in particular, it is desirable to make degradation of data holding characteristics thinner than 4 nm in a meaning, such as to keep step with a direction on the other hand, so that it may explain in full detail later. In this MONOS type, it functions as a charge storage layer which the middle silicon nitride film 18 described above, and an electric charge is accumulated in this trap. The gate electrode 14 comprises a polycide film etc. which, for example, made the silicide film (for example, WSi) laminate on a polysilicon film and a polysilicon film.

[0021]The sidewall 22 which consists of silicon oxide films etc., for example is formed in the both sides of ONO film 12 and the gate electrode 14. The low-concentration impurity diffusion region (n^- field 24) called LDD, respectively is shallowly formed in the substrate face side applied outside from the both edges of the tunnel oxide film 16. On the other hand, the high-concentration impurity diffusion region (n^+ field 26) called sauce or a drain area, respectively is deeply formed in the substrate back side applied outside from the rim of the sidewall 22.

[0022]Although not illustrated in particular, on this, multilevel interconnection of the wiring layers, such as aluminum, is carried out via a layer insulation layer, and the gate electrode 14, sauce, or the n^+ field 26 as a drain area is connected to this multilevel interconnection. Thereby, the interconnection of the memory transistor by word line WLm-1 shown in drawing 2, WLm, WLm+1, bit line BLn-1, BLn, BLn+1, and the common source line SRL is made.

[0023]In such a MONOS type memory transistor of composition, the depression transistor by which the channel was formed in the substrate face on both sides of the tunnel oxide film 16 at the time of no bias is used. The data writing impresses predetermined bias to the gate electrode 14 or the n^+ field 26, and is performed. For example, if pulse voltage is impressed to the word line WLm and the bit line BLn on conditions which were illustrated to drawing 2 when writing data in the central memory transistor MTm and n, an electric charge (in this case, electron) will be supplied to the n^+ field 26 of drawing 3 from the common source line SRL. And the electron which had inside of a channel accelerated is becoming a channel hot electron (CHE) in the pinch-off field near the drain, and running through the tunnel oxide film 16, and after being poured into the silicon nitride film 18 as a charge storage layer, it is accumulated in the trap. The amount of charge storages is decided by the voltage and applying time of pulse voltage.

[0024]According to this amount of charge storages, the threshold voltage Vth of a memory transistor shifts to a right side, and a memory transistor changes to an enhancement mode. As mentioned above, the memory transistor concerning this invention is multiple-value-ized more than ternary. Drawing 4 illustrates the case where the data of four values is memorized in a memory transistor. This figure is a distribution map of the threshold voltage Vth in the memory cell array 4, and a horizontal axis shows the number (frequency) of the memory transistor in which Vth of a vertical axis is the same for Vth.

[0025]If the memory transistor group of the depletion mode in which the electric charge is not accumulated is set to "0" like a graphic display, the memory transistor group "1" of an enhancement mode, "2", and "3" are discretely distributed in order in the direction to which the amount of charge storages increases and Vth becomes high. Usually, in order to make distinction of data easy, like a graphic display, the keepout area of writing is set up between each distribution, and data writing is performed with the margin to this keepout area. Thus, the writing (adjustment of the amount of stored charge) of exact data is attained by carrying out close control of the Vth by said verification circuit in the case of the above-mentioned data writing, verifying the value.

[0026]On the other hand, the bottom of the predetermined bias condition which is not illustrated in particular in this NOR type cell at the time of that data erasure and stored charge are FN(s) (Fowler Nordheim). It is drawn out by the tunnel ring. By the way, as previously pointed out as a problem of conventional technology, by drawing 5 in EEROM. When the electric charge once accumulated in the charge storage layer (for example, silicon nitride film 18) is neglected for a long time, according to a heat-dissipation model, it escapes to the substrate side gradually by stress, and there is a problem that a charge storage characteristic deteriorates.

[0027]In order to cope with this problem, it has some means for compensating this characteristic degradation, and comprises the flash EEPROM 2 concerning this invention. Namely, as shown in drawing 1, in the peripheral circuit 6, The threshold fluctuation detecting circuit 30 as a detection means to detect change of the threshold voltage Vth of a memory transistor, The timer 32 for this threshold fluctuation detecting circuit 30 to give the timing which detects change of Vth, When the threshold fluctuation detecting circuit 30 detects Vth change of a memory transistor, the rewrting circuit 34 as a rewrting means to perform data writing for the second time to a memory cell is formed.

[0028]when operation of this degradation compensation was explained in more detail, the detection timing signal S1 which directs change detection of Vth to the threshold fluctuation detecting circuit 30 called it once from the timer 32 first in the moon, for example -- it is outputted periodically or un-periodically. Whenever it switches on a power supply, for example, it is made to make the detection timing signal S1 output as an example in the case of being un-periodical, or the existence of rewriting is supervised, and when time no rewriting to be exceeds predetermined time, it may be made to make the detection timing signal S1 output. Store beforehand in the memory the table showing a relation with the longest charge holding time (marginal retention time) that serves as

rewriting frequency and a limit of data distinction, for example, and the frequency of rewriting is supervised, If rewriting frequency is large, the detection timing signal S1 will be made to output a little early, and as long as rewriting frequency is small, it may be made to delay the stage to which the detection timing signal S1 is made to output, referring to the read table. You may make it control the processings in these cases of being un-periodical (surveillance about a power supply or rewriting, read-out of a table, etc.) not only by the timer 32 side but by the threshold fluctuation detecting circuit 30 side. In this case, the detection timing signal S1 is a signal of a hour entry.

[0029]By the input of the detection timing signal S1, the threshold fluctuation detecting circuit 30 performs change detection of the threshold voltage Vth of the specific transistor to the memory cell array 4. That is, as shown in drawing 2, the detection start signal S2 is outputted to a specific transistor, and change of the Vth is inputted as the detecting signal S3.

[0030]The reference cell which receives stress equivalent to a memory cell concrete, for example is beforehand provided in the memory cell array 4, and Vth of the reference transistor is seen whether have shifted or not. When the area of the memory cell array 4 is large, a reference cell may be provided for every block which constitutes the memory cell array 4, for example, or word line sector. It may be made to detect a gap of Vth about a regular memory transistor, without providing a reference cell. Specification of the regular memory cell to detect is arbitrary like arrangement of a reference cell.

[0031]Since Vth is shifted to a negative side because stored charge (electron) falls out in order to detect a gap of this Vth, As shown in drawing 4, to threshold distribution of voltage "1", "2", and "3", the detection part of deltaVth width is set to that negative voltage side, and the existence of the specific transistor with which Vth enters in this prescribed width is detected. This detection part is arbitrary, and although it may set up to which threshold distribution of voltage, since it is thought that the amount of change of the distribution "3" by the side of high Vth with many amounts of stored charge is large, generally it is good to set and set prescribed distance to the negative voltage side of the distribution "3" by the side of high Vth. The position of the detection part over Vth distribution can be provided in the positive voltage side edge of a keepout area, for example like a graphic display, although there is no limitation in particular.

[0032]Thus, if it judges that Vth change had the threshold fluctuation detecting circuit 30, from the threshold fluctuation detecting circuit 30, rewrting start signal S4 will be outputted to the rewrting circuit 34. The rewrting circuit 34 which inputted rewrting start signal S4 applies the re-writing of data to the memory cell array 4, as shown in drawing 1.

[0033]Although this re-writing may follow all the memory cells, it may follow only some memory cells. For example, when monitoring a reference cell, only about the memory cell of the circumference of a reference cell with Vth change, it is prescribed units, such as a block and a word line sector, and the re-writing of data may be performed. In the case where a regular memory cell is monitored, only the monitored memory cell besides a prescribed unit may perform the re-writing of data.

[0034]Stored data is once eliminated and the re-writing of this data is usually performed by writing in an initial data again. There is also the method of performing without eliminating stored data. That is, since threshold voltage can be verified for every bit and it can usually control by a multi level memory precisely, it is also possible to return data so that the changed charge quantity of the threshold voltage of a memory transistor may be compensated without performing elimination of stored data. These data re-writing can perform degradation compensation of a charge storage characteristic easily.

[0035]Thus, since degradation of a charge storage characteristic is intense compared with the case where a charge storage layer is a conducting film in the MONOS type (or MNOS type) whose charge storage layers are insulator layers, such as a silicon nitride film, the effect of the degradation compensation by application of this invention is large. This invention is not limited to the above-mentioned explanation.

[0036]For example, in the above-mentioned explanation, the cell method illustrated the case where it had a MONOS type memory transistor with a NOR type, and it was presupposed that electric charge pouring is based on a channel hot electron (CHE). However, electric charge pouring according to NF tunneling with a NAND type or a DINOR type especially for reasons of low power consumption is also possible. Direct tunneling may be used for voltage lowering.
[0037]The thrust omission of the electric charge shifted to direct tunneling from NF tunneling, and this invention persons checked that the changing direction of Vth could be arranged with one side in the range in which the thickness is 3-4 nm, when thickness of the above mentioned tunnel oxide film 18 was made thinner than 4 nm. When an electron falls out, an electron hole does not go into a charge storage layer from the substrate side, and it is thought of because a depression field is not formed at the time of bias application for this reason that the changing direction of Vth can be arranged with one side in this thickness range.
[0038]This means that Vth change of the distribution "0" by the side of low Vth is almost lost by drawing 4. Since this is in agreement with the compensation direction of threshold voltage also for the surrounding memory cell if the changing direction of threshold voltage is beforehand arranged with one side even if there is what is called soft light in which the memory cell connected to the circumference on the occasion of data writing receives influence, it is desirable in this meaning.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

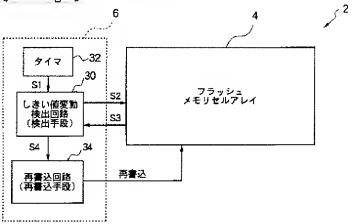
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is an outline lineblock diagram showing the important section about the flash EEPROM concerning this invention.
[Drawing 2]It is a circuit diagram employable as the flash EEPROM of drawing 1 expanding and showing a part of NOR type flash memory cell array.
[Drawing 3]It is an abbreviated section structure figure of a MONOS type memory transistor employable as the flash EEPROM of drawing 1.
[Drawing 4]In the flash EEPROM of drawing 1, it is a distribution map of the threshold voltage (Vth) in the memory cell array in the case of memorizing the data of four values in a memory transistor as an example of multiple-value-izing.
[Drawing 5]It is a figure showing the holding property of the electric charge accumulated into the silicon nitride film about a MONOS type flash EEPROM for problem explanation of conventional technology.
[Description of Notations]
2 -- A flash EEPROM (nonvolatile storage), 4 -- Flash memory cell array, 6 [-- Gate electrode,] -- A peripheral circuit, 10 -- A semiconductor substrate, 12 -- An ONO film, 14 16 -- A tunnel oxide film, 18 -- A silicon nitride film (charge storage layer), 20 -- Upper oxide film, 22 -- A sidewall, 24 -- An n^- field, 26 -- Sauce or the n^+ field as a drain area, 30 -- A threshold detector circuit (detection means), 32 -- A timer, 34 -- Rewrting circuit (rewrting means), MTm, n, etc. -- A memory transistor, WLm-1, WLm, and WLm+1 -- A word line, BLn-1, BLn, and BLn+1 -- [-- A detection timing signal S2 / -- A detection start signal S3 / -- A detecting signal, S4 / -- Rewrting start signal.] A bit line, SRL -- A common source line, S1

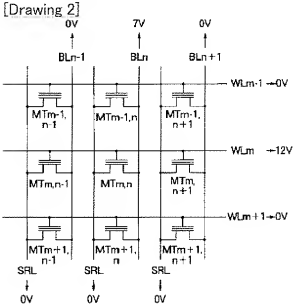
[Translation done.]

DRAWINGS

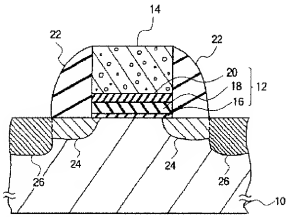
[Drawing 1]



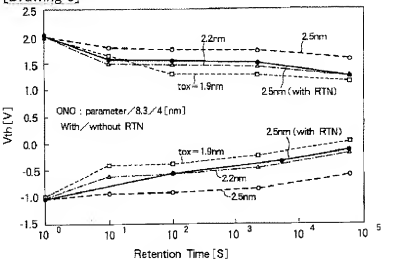
[Drawing 2]



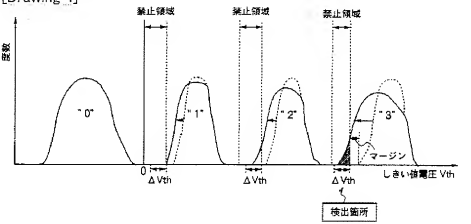
[Drawing 3]



[Drawing 5]



[Drawing 4]



[Translation done.]